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⑦① Applicant: **SGS-THOMSON MICROELECTRONICS, INC.**
(a Delaware corp.)
1310 Electronics Drive
Carrollton, TX 75006 (US)

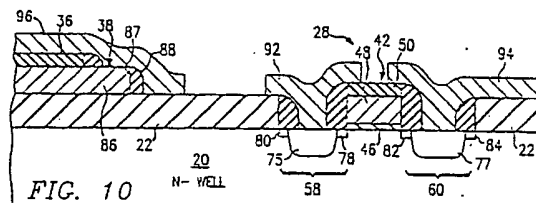
⑦② Inventor: **Chan, Tsiu Chiu**
Cabinet **BALLOT-SCHMIT** 84 avenue Kléber
F-75116 Paris (FR)

Han, Yu-Pin
Cabinet **BALLOT-SCHMIT** 84 avenue Kléber
F-75116 Paris (FR)

⑦④ Representative: **Ballot, Paul Denis Jacques**
Cabinet **Ballot-Schmit** 84, avenue Kléber
F-75116 Paris (FR)

⑤④ **Method for forming a self-aligned source/drain contact for a MOS transistor.**

⑤⑦ A process for forming an MOS transistor with self-aligned contact holes comprises first forming a conductive layer of material over the substrate followed by formation of a capping layer of oxide over the conductive layer. The conductive layer and capping oxide layer are then patterned to form the gate electrode of a transistor with source/drain regions defined on either side thereof. A conformal layer of oxide is then disposed over the substrate and anisotropically etched to remove the oxide layer from the horizontal surfaces leaving a sidewall oxide layer on all substantially vertical surfaces. Thereafter, a second layer of conductive material is deposited over the substrate and patterned to form contacts.



Description

METHOD FOR FORMING A SELF-ALIGNED SOURCE/DRAIN CONTACT FOR AN MOS TRANSISTOR

TECHNICAL FIELD OF THE INVENTION

The present invention pertains in general to forming contacts in an integrated circuit and, more particularly, to a method for forming the contact to the source and the drain regions of an MOS transistor.

BACKGROUND OF THE INVENTION

Conventional MOS FET devices are typically comprised of a gate electrode overlying a channel region and separated therefrom by a gate oxide. Conductive regions are formed in the substrate on either side of the gate electrode and the associated channel to form the source and drain regions. However, the major portion of the source and drain regions is utilized to provide a conductive path to the source and drain junctions. The dimensions of the source and drain regions are a function of the design layout and the photolithographic steps required to align the various contact masks, the alignment tolerances, etc.

Conventionally, an MOS transistor is fabricated by first forming the gate electrode and then the source and drain regions followed by depositing a layer of interlevel oxide over the substrate. Contact holes are then patterned by a separate mask and contact holes cut through the interlevel oxide to expose the underlying source and drain regions. This separate mask step requires an alignment step whereby the mask is aligned with the edge of the gate electrode which is also the edge of the channel region. There is, of course, a predefined alignment tolerance which determines how far from the edge of the gate electrode the ideal location of the contact. For example, if the alignment tolerance were 1 micron, this would mean that the contact wall would be disposed one micron from the edge of the gate electrode on one side and one micron from the edge of the nearest structure on the opposite side thereof. This therefore results in a source or drain region having a dimension of two microns plus the width of the contact. The overall width is therefore defined by alignment tolerances, the width of the conductive interconnection and the minimal separation from adjacent structures. This therefore results in a significant amount of surface area dedicated primarily to mask alignment.

When MOS devices are utilized in a complementary configuration such as CMOS devices, the additional space required to account for alignment tolerances becomes more of a problem. This is due to the fact that CMOS devices inherently require a greater amount of substrate and surface area than either functionally equivalent N-or P-channel FET devices. For example, the CMOS device density in an integrated circuit can be up to 40% less than the device density achieved by using conventional NMOS technology.

This size disadvantage is directly related to the amount of substrate surface area required for

alignment and processing latitudes in the CMOS fabrication procedure to insure that the N- and P-channel transistors are suitably situated with respect to the P-well. Additionally, it is necessary to isolate the N-and P channel transistors from each other with fixed oxide layers with an underlying channel stop region. As is well known, these channel stops are necessary to prevent the formation of parasitic channels between neighboring transistors. Typically, the channel stops are highly doped regions formed in the substrates surrounding each transistor and effectively block the formation of parasitic channels by substantially increasing the substrate surface inversion threshold voltage. Also, they are by necessity the opposite in conductivity type from the source and drain regions they are disposed adjacent to in order to prevent shorting. This, however, results in the formation of a highly doped, and therefore, low reverse breakdown voltage P-N junctions. Of course, by using conventional technology with the channel stops, there is a minimum distance by which adjacent transistors must be separated in order to prevent this parasitic channel from being formed and to provide adequate isolation.

SUMMARY OF THE INVENTION

The present invention disclosed and claimed herein comprises a process for forming self-aligned contacts extending from a second and upper structural level to a first and lower structural level on a substrate. The process includes first forming a conformal layer of conductive material at the first structural level and then forming a cap layer of insulating material over the surface of the conducting layer. The combined conducting layer and insulating layer are then patterned and etched to define a conductive structure with the insulating layer forming a protective cap on the surface thereof, the conductive structure having at least one substantially vertical surface. A sidewall insulating layer is then formed on the substantially vertical surface of the conductive structure to a predetermined thickness. The outer surfaces of the sidewall insulating material form the contact hole or via. A second layer of conductive material is then formed in the second structural level and insulated from the first conductive layer by the protective cap layer of insulating material. The second layer of conductive material is then patterned and etched to define a conductive pattern at the second level.

In another embodiment of the present invention, the first structural level has at least one active region, the active region being surrounded by a layer of thick insulating material. The conductive structure is comprised of a transistor gate which is separated from the surface of the active region by a layer of gate insulating material. The gate electrode has two substantially vertical surfaces which each have a layer of sidewall insulating material disposed thereon. A light dosage of impurities of conductivity

type opposite to that of the substrate is introduced into the surface of the substrate prior to the formation of the sidewall insulating layers. After formation of the sidewall insulating layers, a heavy dose of impurities of a conductivity type opposite to that of the substrate is then introduced into the substrate to form heavy implant portions of the source/drains of the transistor. The second layer of conductive material is then deposited and patterned to form the source/drains of the transistor.

In yet another embodiment of the present invention, the thick insulating layer and the active regions are formed by first forming a thick layer of field oxide over the substrate and then patterning the field oxide layer to form the active regions. The thick oxide layer is etched to form the active regions such that the boundaries of the active regions at the thick oxide layer comprise substantially vertical surfaces of insulating material. The substantially vertical surfaces are covered with the sidewall insulating layer at the same time the substantially vertical surfaces of the gate electrodes are covered with the sidewall insulating layer. Therefore, the light dosage of impurities extends under the sidewall insulating layer whereas the heavy implant portions are spaced away from the substantially vertical surfaces of the thick oxide layer.

In a further embodiment of the present invention, the cap layer of insulating material is patterned and etched down to the surface of the first layer of conductive material to expose the surface thereof at preselected locations. Thereafter, the second layer of conductive material can directly contact the surface of the first layer of conductive material without requiring a separate contact hole pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying Drawings in which:

Figure 1, illustrates a cross-sectional diagram of the initial substrate after the N- and P-well implants;

Figure 2 illustrates a cross-sectional diagram of a substrate after the N- and P-well implants have been driven down to form the N- and P-wells;

Figure 3 illustrates a cross-sectional diagram of the substrate of Figure 2 with a layer of thick oxide grown over the substrate and patterned to form the active areas;

Figure 4 illustrates a cross-sectional diagram of the substrate of Figure 3 after etching the active area and adjusting the V_T in the P-well;

Figure 5 illustrates a cross-sectional diagram of the substrate of Figure 4 with a layer of polycrystalline silicon conformally coating the substrate followed by an upper layer of oxide;

Figure 6 illustrates a cross-sectional diagram of a portion of the substrate of Figure 5 after patterning and etching the gate electrodes and lightly implanting the source and drain regions;

Figure 7 illustrates a cross-sectional diagram

of the substrate of Figure 6 with a layer of conformal oxide deposited over the substrate;

Figure 8 illustrates a cross-sectional diagram of the substrate of Figure 7 after anisotropically etching the oxide layer and implanting the source/drain regions;

Figure 9 illustrates a cross-sectional diagram of the substrate of Figure 8 after depositing the second conductive layer of silicide over the substrate;

Figure 10 illustrates a cross-sectional diagram of the substrate of Figure 9 after patterning and etching of the second conductive layer;

Figure 11 illustrates a top view of one transistor in the substrate of Figure 10;

Figure 12 illustrates a schematic diagram of a 6-T static ram cell;

Figure 13 illustrates a top view of the 6-T cell of Figure 12 fabricated utilizing the process of the present invention; and

Figures 14 and 15 illustrate a cross-sectional diagram and perspective view, respectively, of the metal level to second conductive level interconnect.

DETAILED DESCRIPTION OF THE DESCRIPTION

Referring now to Figure 1, a silicon substrate 10, which in the preferred embodiment, is prepared for use in a CMOS process. The substrate 10 has an N-well and a P-well region defined thereon. The P-well region is generally referred to by the reference numeral 12 and the N-well is generally referred to by the reference numeral 14. Thereafter, the substrate is patterned with a protective nitride cap (not shown) over the P-well 12, and then N-type impurities implanted into the N-well region 14. The substrate is then subjected to a steam oxidation step to grow a thick layer of oxide 16 over the N-well region 14. The nitride cap (not shown) is then stripped away and P-type impurities implanted into the P-well region 12. The energy of the P-well implant is insufficient to go through the oxide layer 16.

Referring now to Figure 2, after implanting of the P-well region 12 and the N-well region 14, the implanted impurities are driven down into the substrate 10 to form a P-well 18 and an N-well 20. The layer of oxide 16 is then stripped off.

Referring now to Figure 3, after formation of the P-well 18 and N-well 20, the substrate is subjected to a steam oxidation process and a thick layer of oxide 22 is grown over the entire substrate 10 to a thickness of approximately 5,000 Å. A layer of photoresist 24 is then deposited on the substrate and patterned to form an active region 26 over the P-well 18 and an active region 28 over the N-well 20.

Referring now to Figure 4, the substrate 10, after patterning, is subjected to a plasma etch whereby the portions of the oxide layer 22 in the active regions 26 and 28, respectively, are removed down to the surface of the substrate, resulting in substantially vertical walls bounding the active regions. A thin layer of gate oxide is then deposited or grown over the substrate to a thickness of approximately 200 Å, resulting in a layer of gate oxide 30 in the active region 26 and a layer of gate oxide 32 in the

active region 28. The N-well region 14 is then masked off (not shown) leaving P-well 18 open and then N-channel transistor threshold voltage adjust impurities implanted into the active region 26 to adjust the threshold of active devices formed therein.

Referring now to Figure 5, after the threshold adjust in the P-well 18, a layer of polycrystalline silicon 34 is deposited over the substrate to form a conformal layer which has a thickness of approximately 4,000 Å. The poly layer 34 is then doped with N-type impurities to increase the conductance thereof. A layer of oxide 36 is then deposited over the poly layer 34 to a thickness of approximately 2,000 Å. For reasons described hereinbelow, the upper surface of the oxide layer 36 is patterned to provide an opening 38 therein to expose the underlying polysilicon layer 34 in a region overlying the thick oxide layer 22. However, the opening 38 can also be disposed over one of the active regions 26 or 28, as will be described hereinbelow.

Referring now to Figure 6, the additional steps required to form a transistor in each of the active regions 26 and 28 will be described with reference only to the formation of a transistor in the active region 28 in N-well 20. For illustrative purposes, an additional active region 40 is illustrated in the N-well 20 which was not illustrated in Figures 3-5. After the layer of poly 34 has been formed with the protective oxide layer 36 on the upper surface thereof, gate electrodes are patterned and formed with a gate electrode 42 formed in the active region 28 and a gate electrode 44 formed in the active region 40. The gate electrode 42 is comprised of a layer of gate oxide 46 formed from the oxide layer 32, a layer of doped polycrystalline silicon 48 formed from the poly layer 34 and a capping layer of protective oxide 50 formed from the oxide layer 36. Similarly, the gate electrode 44 is comprised of a gate oxide layer 52, a poly layer 54 and a protective oxide layer 56.

From a dimensional standpoint, the gate electrodes 42 and 44 are each approximately 0.8 microns in width, corresponding to the channel length of 0.8 microns with the source and drain regions defined on either side thereof having a width of approximately 1.0 microns. That is, the distance between the edge of the gate electrode to the edge of the oxide layer 22 is approximately 1.0 microns, this region being the available space within which to make contact to. As will be described hereinbelow, with the process of the present invention, the portion of the oxide layer 22 isolating the two active regions 28 and 40 can be as small as 1.0 microns and still provide sufficient isolation.

After formation of the gate electrodes 42 and 44, a light dosage of P-type impurities are implanted into the exposed region of the substrate on either side of the electrodes 42 and 44. The P-type impurities, in the preferred embodiment, are Boron and are implanted to a dosage of approximately 1×10^{13} ions/cm², resulting in an implanted layer after an annealing step with a thickness of approximately 0.15 microns. During this implantation step, the portion of the substrate 10 in which the P-well 18 was formed is masked off with a subsequent implant

step of N-type impurities utilized to form the lightly doped source and drain regions for the transistors to be formed therein. This results in source/drain regions 58 and 60 being formed in the active region 28 on either side of gate electrode 42 and a source/drain region 62 being formed in the active region 40, the other source/drain region not being illustrated.

Referring now to Figure 7, after formation of the source/drain regions 58-62, a conformal layer of oxide 64 is deposited over the substrate to a thickness of approximately 3,000 Å. It is important to note that the thickness of the oxide over the poly portion 48 of the electrode 42 and the poly portion 54 of the electrode 44 is now approximately 5,000 Å, due to the thickness of the oxide layers 50 and 56, which were formed from the oxide layer 36, illustrated in Figure 5.

Referring now to Figure 8, after formation of the oxide layer 64 over the substrate, the surface of the structure on the substrate 10 is then subjected to an anisotropic etch. For illustrative purposes, only the active region 28 and the transistor formed therein will be described. The anisotropic etch is substantially unidirectional and etches primarily in the vertical direction with the oxide on any substantially vertical surfaces remaining. This results in a layer of sidewall oxide disposed on all vertical surfaces to a thickness of approximately 3,000 Å. As described above, since only 3,000 Å of oxide was disposed over the substrate, it is only necessary to etch the surface for a duration of time sufficient to remove 3,000 Å of oxide. This will allow at least a portion of the capping protective oxide layer 50 to remain over the poly layer 48 of gate electrode 42. This results in a layer of sidewall oxide 66 being formed over the vertical surface of the portion of the thick oxide layer 22 adjacent the source/drain region 58, a layer of sidewall oxide 68 disposed over the vertical surface of the gate electrode 42 adjacent the source/drain region 58, a layer of sidewall oxide 70 disposed over the vertical surface of the portion of the thick oxide layer 22 adjacent the source/drain region 60 and a layer of sidewall oxide 72 disposed over the vertical surface of the gate electrode 44 adjacent the source/drain region 60. Since each of the source/drain regions 58 and 60 initially had a width of approximately 1.0 micron, the distance between the outer surfaces of the sidewall oxide layers 66, 68, 72 and 70 respectively, is approximately 0.25 microns. This results in a contact opening 74 being formed over the source/drain region 58 and a contact opening 76 being formed over the source/drain region 60 contact openings 74 and 76 dimensioned to be approximately 0.5 microns.

After formation of the contact openings 74 and 76 over the source/drain regions 58 and 60 respectively, a heavy dosage of P-type impurities is then implanted through the openings 74 and 76. The dosage is approximately 2×10^{15} ions/cm² of a Boron impurity at an energy sufficient to form source/drain heavy implant regions 75 and 77 with each region 75 and 77 having a thickness of approximately 0.3 microns after a subsequent annealing and drive step. It should be noted that during the drive step

there is some lateral movement of the heavy dosage implants. This results in a heavy implant with a light reach-through implant on both sides of the source/drain region. The source/drain region 58 has a reach-through implant region 78 to connect the heavy implant region 75 to the channel region underlying the gate electrode 42 and a light implant region 80 formed on the opposite side of the heavy implant region 75 to connect the heavy implant region 75 to the edge of the thick oxide layer 22. In a similar manner, the source/drain region 60 has a lightly implanted reach-through implant region 82 disposed between the heavy implant region 77 and the edge of the channel region underlying the gate electrode 42, and a reach-through implant region 84 for connecting the heavy implant region 77 to the edge of the thick oxide layer 22. As will be described hereinbelow, the reach-through implant regions 80 and 84 are useful in the isolation of adjacently disposed transistors. The lightly doped regions 78 and 82 are functional to form a lightly doped drain (LDD) transistor.

Referring now to Figure 9, there is illustrated a detail of the active region 28 and the opening 38 in the oxide layer 36 illustrated in Figure 5. It can be seen that during patterning of the poly layer 34 to form the gate electrodes 42 and 44, a portion 86 is also formed from the poly layer 34 which is utilized to provide interconnections with other structures on the substrate, over which the opening 38 is formed. It should be noted that the portion 86 is formed within the opening 38 such that an edge 87 is exposed. In accordance with the previously described process steps, the portion of the oxide layer 36 on the inside of the opening 38 has a sidewall oxide layer formed on the vertical surfaces thereof in addition to a sidewall oxide layer 88 formed over the edge 87 of the portion 86 of the poly layer 34 for isolation purposes.

After implanting of the source/drain regions 58 and 60 and subsequent implantation of the source/drain regions (not shown) in the P-well 18, a second conductive layer of silicide 90 is deposited on the substrate to form a conformal layer which has a thickness of approximately 4,000 Å. The silicide layer 90 is formed by conventional techniques utilizing either a deposited silicide such as tantalum silicide or forming the silicide after deposition of a refractory metal layer such as titanium to form TiSi₂. The second conductive layer of silicide 90 contacts the substrate in the contact openings 74 and 76 and also contacts the surface of the first layer of poly 34 on the portion 86 through opening 38. Therefore, contact openings which were formed through the use of the sidewall oxide layers are fabricated in a single step to expose both the surface of the silicon and select surfaces of the first layer of poly. The oxide layer 36 which formed the oxide layer 50 on the gate electrode 42 provides an important function of selectively isolating the upper surfaces of the first layer of poly 34, with the sidewall oxide layers isolating the vertical surfaces. Thus, a self-aligned step is provided which requires no additional patterning and associated alignment step to open the contact holes. This is an important aspect of the

present invention.

From an alignment standpoint, the mask utilized to pattern gate electrode 42 and the mask utilized to fabricate a conventionally formed contact hole are typically aligned with the same alignment mark. If the gate electrode 42 is misaligned for any reason in one direction and the contact hole is misaligned in the opposite direction, a cumulative error results. This error must be accounted for by providing additional space between the edge of the gate electrode and the edge of the active region. However, utilizing the process of the present invention, the spacing provided by the sidewall oxide layers 70 and 72, which sidewall oxide layers are self-aligned with respect to the edge of the gate electrode 42, no alignment step is required, thus allowing the contact hole to be spaced away from the edge of the gate electrode 42 by a smaller distance.

Referring now to Figure 10, after depositing the silicide layer 90 over the substrate, the layer 90 is patterned and etched to form a contact 92 to the region 75 of the source/drain region 58, a contact 94 to the region 77 of the source/drain region 60 and a contact 96 to the portion 86 of the first layer of poly 34. It should be understood that the gate electrode 42 can extend back over the substrate and be contacted by the second layer of silicide 90 in a similar manner to the method by which the contact 96 contacts the portion 86. In addition, it should be noted that the contact 96 overlaps the portion 86 and sidewall oxide layer 88.

It can be seen that after formation of the contacts 92 and 94 between the second level silicide layer 90 and the source/drain regions 58 and 60, respectively, the contacts are spaced away from the gate electrode 42 by a predefined distance in addition to being spaced away from the vertical wall of the thick oxide layer 22 by the same predefined distance. This predefined distance is the thickness of the sidewall oxide layer. Since the reach-through implant or light dosage of impurities was introduced into the substrate 10 prior to formation of the sidewall oxide layers 66-72, the result is that the contacts 92 and 94 and the source/drain heavy implant regions 75 and 77 are spaced a predetermined distance from both gate electrode 42 and from the thick oxide layer 22. With respect to the transistor, this forms the increased breakdown voltage of the well-known LDD transistor. However, it can be seen that a thick field transistor is also formed which is an LDD transistor. One parameter that is important in an integrated circuit is the threshold voltage of the thick field transistor. With the process of the present invention, it is possible to provide more closely spaced transistors while insuring that the contacts and the heavy implant are spaced away from the edge of the thick oxide layer 22 by a predetermined distance and from the edge of the gate electrode 42 by a predetermined distance. For example, the alignment mask for the active region and the thickness of the sidewall oxide layer determine the distance that the contact 60 is spaced away from the gate electrode 42.

Referring now to Figure 11 there is illustrated a top view layout of the transistor formed in active

region 28 on the substrate 10, wherein like numerals refer to like parts in the various figures. It can be seen that the gate electrode 42 runs over the substrate and extends up over the oxide layer 22 to form a contact pad 98 on one end thereof similar to portion 86. A contact opening 100 is formed over the contact pad 98 through the oxide layer 36 which covers the gate electrode 42 to expose the underlying polycrystalline silicon. The contact opening 100 is formed by the same process utilized to form the opening 38. It should be understood that the dimensions of this contact opening 100 are a result of an initial contact opening having the vertical surfaces thereof covered by approximately 3,000 Å of sidewall oxide.

As illustrated in Figure 11, the contact area 100 is greater than the dimensions of the contact pad 98, and, therefore, overlaps the contact pad. This is distinctly different from the situation where the contact was smaller than the overall dimension of the contact pad. This was typically referred to as a "dog-bone" structure. With the process of the present invention, the size of the contact opening 100 which corresponds to the contact opening 38 in Figures 1-10, defines the actual conductive opening or potential conductive opening to which the structure in the second level silicide 90 can contact through. It is therefore not necessary to have a contact pad that is larger than the contact opening itself, thus decreasing the amount of space that must be dedicated to the contact pad.

The contact openings 74 and 76 are illustrated in phantom lines, which phantom lines represent the spacing distance from the edge of the gate electrode 42 and the edge of the thick oxide layer 22. It can be seen that the location of the edges of the contact openings 74 and 76 are a function only of the relative alignment of the mask utilized to form the gate electrode 42 and the mask utilized to form the initial openings defining the active areas 26 and 28. However, the distance from the edge of the gate electrode 42 to the edge of the contact openings 74-76 and the edge of the thick oxide layer 22 to the edge of the contact openings 74-76 is not mask related. Therefore, because orientation does not affect these dimensions, the actual contact to the underlying silicon is spaced a predetermined distance away from either the insulating thick oxide layer 22 or the gate electrode 42. This is to be compared with prior processes wherein a contact mask was aligned with respect to predetermined alignment marks and any misalignment of the alignment mask with respect to either the first poly layer mask or the mask defining the active regions would result in movement of the contact openings with respect to the edge of the gate electrode 42 and the edge of the thick oxide layer 22.

Referring now to Figure 12, there is illustrated a schematic of a six transistor static memory cell which is fabricated utilizing the process of the present invention. The static memory cell is comprised of a CMOS pair with a P-channel transistor 102 and an N-channel transistor 104 having the gates thereof tied together and the drain of the P-channel transistor 102 and the drain of the

N-channel transistor 104 being connected to an output node 106. A second CMOS pair having a P-channel transistor 108 and an N-channel transistor 110 is provided with the gates thereof tied together, and the drain of the P-channel transistor 108 and the drain of the N-channel transistor 110 connected to a node 112. The gates of the first CMOS pair are connected to the node 112 and the gates of the second CMOS pair are connected to the node 106. The sources of both N-channel transistors 104 and 110 are connected to ground and the sources of both P-channel transistors 102 and 108 are connected to the supply voltage V_{cc} . A transfer N-channel transistor 114 is provided with the source-to-drain path thereof connected between the node 106 and an output with the gate thereof connected to a transfer signal. A second N-channel transfer transistor 116 is provided having the source-to-drain path thereof connected between node 112 and an output terminal with the gate thereof connected to the transfer signal.

Referring now to Figure 13, there is illustrated a layout of the 6-T cell of Figure 12 utilizing the process of the present invention. The P-channel transistor 102 has a source 118 and a drain 120 and the P-channel transistor 108 has a source 122 and a drain 124. The sources 118 and 122 are connected together through a common region 126 formed during the source/drain implant of the P-channel transistors 102 and 108. In a similar manner, the N-channel transistor 104 has a source 128 and a drain 130 and N-channel transistor 110 has a source 132 and a drain 134. The N-well is defined by a border 136.

The gates of the P-channel transistor 108 and the N-channel transistor 110 are formed with a single run of polycrystalline silicon 138 which is formed from the first level of poly. In a similar manner, the gates of the P-channel transistor 102 and the N-channel transistor 104 are formed from a second run of polycrystalline silicon 140 formed from the first layer of poly. The poly run 138 extends over the channel region to form the gate electrode of the transistor 108 and also over the channel region in the transistor 110 to form the gate electrode therein. An interconnecting portion 142 extends outward from the run 138 and has a contact opening 144 formed in the end thereof. An interconnecting portion 146 extends outward from the run 140 and has a contact opening 148 disposed in the end thereof. The contact openings 144 and 148 represent openings in the protective oxide layer covering the poly runs 138 and 140 and the interconnecting portions 142 and 146. This protective oxide covers the entire layer of poly in the first level poly.

The drain of P-channel transistor 102 has a self-aligned contact opening 150 formed thereto in accordance with the present invention described above and the drain 124 has a self-aligned contact opening 152 formed thereto. In a similar manner, the drain of N-channel transistor 104 has a self-aligned contact opening 154 formed thereto and the drain of the N-channel transistor 110 has a self-aligned contact opening 156 formed thereto. It can be seen that the self-aligned contact openings are disposed

away from the edge of the gates and the boundary edges of the thick oxide layer, which boundaries define the source/drain regions.

The interconnects formed between the nodes 106 and 112 and the opposite CMOS pairs are formed in a second level of silicide disposed over the first level of poly and separated therefrom by a combination of the oxide layer over the first level of poly and the sidewall oxide layers formed on the vertical walls in accordance with the present invention. The contact 152 and the contact 156 between the drain of P-channel transistor 108 and the drain of N-channel transistor 110 are connected together by a run of second level poly 160. Additionally, a contact is formed through contact opening 148 to provide connection of the second level silicide 160 with the poly run 146. A second run 162 of second level silicide is provided for connection between the self-aligned contact opening 150 and the self-aligned contact opening 154 for the drain of P-channel transistor 102 and the drain of N-channel transistor 104, respectively, and also for being connected to the contact opening 144 for providing a connection conduction with the poly run 142 in the first level poly.

The N-channel transistors 114 and 116 are fabricated during formation of the first level poly with a run of poly 164, with the source/drain path of transistor 114 connected to the drain 130 of transistor 104 and the source/drain path of transistor 116 connected to the drain of transistor 110. The sources of transistors 104 and 110 are connected together through a run of another metal level, not shown, to ground.

The other side of the source-to-drain paths of transistors 114 and 116 are connected to a metal level interconnect, not shown, to provide the bit line. In order to provide a metal level interconnect, a contact pad 168 fabricated from the second level of silicide is formed over a contact opening 170. The contact opening 170 is formed by the sidewall oxide disposed on the edges of the active region and the edges of the poly run 164 forming the gates of transistors 114 and 116. The contact pad 160 overlaps both the poly run 164 and a poly run 172, the poly run 172 forming the access transistors on another and adjacent 6T cell. The contact pad 168 provides a conductive surface to which the upper metal level interconnect is connected through a contact opening 174. The contact opening 174 represents the ideal contact opening wherein a contact opening is formed through a layer of interlevel oxide (not shown). If, for some reason, there were a misalignment, the contact opening 174 would be biased toward one edge of the contact pad 168. It can be seen that the contact pad 168 increases the available contact area for the metal level interconnect without increasing the area of the source/drain of the transistor underlying the contact pad 168. This is due to the fact that the contact pad 168 can overlie adjacent layers of the first level poly, such as poly run 164 and poly run 172.

The transistor 116 and the source/drain thereof which is provided for contacting the bit line has a contact pad 176 formed similar to the contact pad

168. The contact pad 176 provides the increased contact area for the metal level interconnect and interfaces with a contact opening 178 in the underlying source/drain. A contact opening 180 is provided for contacting the interconnect metal level (not shown).

Referring now to Figures 14 and 15, there is illustrated a cross-sectional diagram and perspective view, respectively, of the portion 168 taken along lines 14-14 in Figure 13 and illustrating the metal level interconnect. The poly run 164 is bounded on either side thereof by sidewall oxide layers 182 with the poly run 172 being bounded on either side thereof by sidewall oxide layers 184. The upper portion of poly run 164 is protected by a protective oxide cap 186 and the upper surface of poly run 172 is protected by a protective oxide cap 188. Layers 186 and 188 are fabricated from the protective oxide layer 36, as illustrated in Figure 4. The channel regions underlying the gates formed with the poly runs 164 and 172 are separated from each other by a common source/drain well 190. The contact 170 is therefore formed between the exterior surface of the sidewall oxide layers 182 and 184 overlying the source/drain 190.

After formation of the contact opening 170, the second level silicide is disposed over the surface and patterned to form the contact pad 168. It can be seen that the contact pad 168 has a significantly larger surface area than the contact opening 170. Thereafter, a layer of interlevel oxide 192 is formed over the surface and then planarized. The contact 174 in the form of a via is formed through the interlevel oxide 192. A layer of metal 194 is then sputtered onto the surface and patterned to form the interconnect at the metal level. It can be seen that the use of the contact pad 168 formed from the second level silicide serves to increase the area to which the contact opening 174 is aligned to. In this manner, the area of the contact opening 170 can be decreased since the portion 168 in effect amplifies the contact 170 at the second level without requiring the increased surface area at the first level.

In summary, there has been provided a process for forming self-aligned contacts which are aligned in one embodiment to the edge of a conductor and in one embodiment to the edge of a vertical surface of the isolation field oxide. The process includes first defining a conductive structure in an active region which has at least one vertical surface. A layer of conformal oxide is then disposed over the substrate and anisotropically etched to form sidewall layers on the vertical surfaces. The conductive structure is initially fabricated with a protective cap of oxide thereon such that the entire conductive structure is encased in a protective oxide. The sidewall oxide layer on the vertical surface forms one surface of the contact via. Thereafter, the contact is formed by depositing a layer of conductive material over the substrate and then patterning it and etching it to form contacts.

Although the preferred embodiment has been described in detail, it should be understood that various changes, substitutions and alterations can be made therein without departing from the spirit

and scope of the invention as defined by the appended claims.

Claims

1. A method for forming contact holes from a first structural level in a semiconductor structure to a second structural level therein, comprising:

forming a layer of conductive material at the first structural level;

forming a capping layer of insulating material over the layer of conductive material at the first structural level to provide a protective insulating layer thereon, the second structural level above the upper surface of the capping layer;

patterning the capping layer and the layer of conductive material to define a predetermined conductive structure having at least one substantially vertical wall;

forming a conformal layer of insulating material over the conductive structure at the first structural level; and

anisotropically etching the conformal insulating layer in a primarily vertical direction down from the second structural level to the first structural level such that the portion of the conformal insulating layer on the substantially vertical walls of the conductive structure are not removed, the step of anisotropically etching leaving a sidewall layer of insulating material and exposing the surface of the first structural level spaced away from the substantially vertical wall by the thickness of the insulating sidewall layer; wherein the portion of the capping layer remaining on the conductive structure and the insulating sidewall layer electrically insulate the conductive portion of the conductive structure; wherein the outer surfaces of the insulating sidewall layer provide the sidewalls of the contact hole that are spaced from the substantially vertical walls of the capped structure by the thickness of the insulating sidewall layer.

2. The method of Claim 1 wherein the step of patterning the capping layer and the layer of conductive material comprises:

defining a pattern on the upper surface of the capping layer of insulating material; and etching the capping layer and layer of conductive material down to the first structural level in accordance with the defined pattern.

3. The method of Claim 1 wherein the capping layer of insulating material and the conformal layer of insulating material comprise silicon dioxide and the semiconductor structure comprises a silicon base material.

4. The method of Claim 3 wherein the first structural level is formed on the surface of the substrate.

5. The method of Claim 4 and further comprising:

forming a layer of thick oxide over the substrate; and

patterning and etching the thick oxide layer to

define isolating portions of the thick oxide layer having substantially vertical walls such that the isolating portions are part of the first structural level;

wherein isolating sidewall layers of the conformal layer of insulating material are formed on the substantially vertical walls of the isolating portions to space the contact hole away from the edge of the isolating portion by the thickness of the isolating sidewall layers.

6. The method of Claim 1 and further comprising:

forming a conformal layer of conductive material over the semiconductor substrate after formation of the contact holes; and

patterning the layer of conductive material to form contacts in the contact holes.

7. The method of Claim 1 and further comprising patterning the capping layer of insulating material and removing the patterned portions thereof to selectively expose regions of the layer of conductive material in the first structural level prior to forming the conformal layer of insulating material such that interlevel contact holes are formed to the surface of the conductive structure.

8. The method of Claim 7 and further comprising:

forming a conformal layer of conductive material over the semiconductor substrate after formation of the contact holes; and

patterning the layer of conductive material to form contacts in the contact holes and in the interlevel contact holes.

9. A process for forming contacts from a second, upper structural level to a first, lower structural level in a semiconductor structure, said semiconductor structure including a semiconductor structure substrate, comprising:

forming a layer of thick oxide over the semiconductor substrate;

patterning the thick oxide layer to define at least one active region on the first level;

forming a conductive structure on at least a portion of the surface of the active region, the conductive structure having at least one substantially vertical wall spaced apart from the edges of the thick oxide layer at the boundary of the active region, the conductive structure having a conductive layer and a capping layer of insulating material overlying the conductive layer, the second structural level being above the capping layer;

forming a sidewall insulating layer on the substantially vertical walls of the conductive structure such that the sidewall insulating layer and the capping layer electrically insulate the top and sides of the conductive layer of the conductive structure;

forming a conformal layer of conductive material at the second structural level and extending down to the first structural level and contacting the exposed surfaces of the active region; and

patterning the conformal layer of conductive

material in accordance with a predetermined pattern to form conductive contacts from the second structural level to the first structural level with the outer surfaces of the sidewall insulating layer forming the boundaries of a contact opening and the capping layer of the conductive structure electrically isolating the conductive layer in the conductive structure from the conformal layer of conductive material.

10. The method of Claim 9 and further comprising:

forming a selective opening in the capping layer on the conductive structure to expose the underlying conductive layer in a predetermined region such that the conformal layer contacts the upper surface of the conductive layer in the conductive structure at the selective opening; and

patterning the conformal layer of material to provide a contact between the second structural level and the upper surface of the conductive layer in the conductive structure through the selective opening.

11. The method of Claim 9 wherein the step of forming the active region surrounded by the thick oxide layer comprises:

forming a layer of thick oxide to a predetermined thickness on the surface of the substrate;

forming a masking layer on the upper surface of the thick oxide layer to define the active region; and

selectively removing the portion of the thick oxide layer overlying the active region defined by the mask to form substantially vertical walls in the thick oxide layer at the boundary of the active region.

12. The method of Claim 11 and further comprising forming a sidewall insulating layer on the substantially vertical walls of the thick oxide layer prior to forming the conformal layer of conductive material at the structural level.

13. The process of Claim 9 wherein the conductive structure further includes a layer of insulating material disposed between the conductive layer and the surface of the active region, and the conductive structure comprises the gate electrode of a transistor having a substantially vertical surface on a source side of the gate electrode and a substantially vertical surface on the drain side of the gate electrode and further comprising:

introducing a light dosage of impurities of the opposite type from the substrate into the surface of the active region on either side of the gate electrode;

the step of forming the sidewall insulating layer on the substantially vertical surfaces of the conductive structure comprising forming the sidewall insulating layer on the substantially vertical surfaces of the gate electrode on both the source and the drain side; and

introducing a high dose of impurities of the opposite conductivity type from the substrate into the active region on either side of the gate

electrode.

14. The method of Claim 13 wherein the method of introducing the light dosage of impurities and the heavy dosage of impurities comprises ion implantation techniques.

15. The method of Claim 9 wherein the step of forming the sidewall insulating layer on the substantially vertical surface of the conductive structure comprises:

forming a conformal layer of oxide of a predetermined thickness over the surface of the active region; and

anisotropically etching the conformal layer of oxide primarily in the vertical direction for a predetermined amount of time required to remove at least the conformal layer of oxide on the horizontal surfaces, such that the capping layer of insulating material in the conductive structure is not completely removed and the exposed surface active region is spaced apart from the substantially vertical surface of the conductive structure by the thickness of the conformal layer of oxide.

16. The method of Claim 9 wherein the step of forming the conductive structure comprises:

depositing a layer of conductive material over the surface of the active region;

forming a layer of insulating material over the conductive layer;

patterning the combined conductive layer and insulating material layer to define the conductive structure; and

etching the combined conductive layer and insulating material layer to form the conductive structure in accordance with a predetermined conductive structure pattern and the conductive structure having at least one substantially vertical surface.

17. The method of Claim 16 wherein the step of forming the conductive layer comprises depositing a layer of silicide over the surface of the active region and the step of forming the layer of insulating material comprises depositing a layer of silicon dioxide over the surface of the active region, the substrate being silicon.

18. A method for forming an MOS transistor in an integrated circuit with self-aligned contacts, comprising:

forming active regions in a substrate, each active region bounded by a thick insulating layer;

forming a layer of gate insulating material over the active region and thick insulating layer;

forming a first and conformal layer of conductive material over the surface of the layer of gate insulating material;

forming a capping layer of insulating material over the first layer of conductive material;

patterning and etching the combined layers of gate insulating material, first layer of conductive material and capping layer of insulating material to form gate electrode in the active region having substantially vertical sidewalls;

introducing a light dose of impurities of opposite conductivity type to the conductivity type of

the substrate into the active region on both sides of the gate electrode to form lightly doped source/drain region;
 forming a layer of sidewall insulating material on the substantially vertical sidewalls of the gate electrode to a predetermined thickness;
 introducing a heavy dose of impurities of a conductivity type opposite to the conductivity type of the substrate into the active region on both sides of the gate electrode to form heavily doped source/drain regions;
 forming a second and conformal layer of conductive material over the gate electrode, active regions, layers of sidewall insulating layers and thick insulating layer that conforms to the topology of the substrate such that the second layer of conductive material contacts the surface of the active region spaced away from the gate electrode by approximately the thickness of the sidewall insulating material;
 and
 patterning and etching the second layer of conductive material in accordance with a predetermined pattern to provide a connective pattern and contacts from a second level above the surface of the substrate to the heavily implanted source/drain regions.

19. The method of Claim 18 and wherein the step of forming active regions comprises:
 forming a layer of thick oxide over the surface of the substrate;
 patterning and etching the thick oxide layer to remove portions thereof overlying the active regions such that the thick oxide layer at the boundaries of the active region has substantially vertical surfaces; and
 the step of forming the layer of sidewall insulating material on the substantially vertical surfaces on the gate electrode also forms a sidewall insulating layer on the substantially vertical surfaces of the thick oxide layer after patterning and etching thereof.

20. The method of Claim 18 wherein the gate insulating material and the capping layer of insulating material are oxide and the first layer of conductive material is doped polycrystalline silicon.

21. The method of Claim 18 wherein the step of forming the layer of sidewall insulating material comprises:
 forming a conformal layer of oxide over the gate electrode, active regions and thick insulating layer; and
 anisotropically etching the conformal layer of oxide to remove portions of the conformal layer of oxide on horizontal surfaces to leave the portions of the conformal layer on vertical surfaces substantially unetched;
 wherein the step of anisotropically etching is stopped when the thickness of the conformal layer of oxide is removed such that only minimal removal of the portion of the capping layer of insulating material remaining on the gate electrode is removed.

22. The method of Claim 18 and further

comprising:

removing a selected region of the capping layer of insulating material to expose the surface of the underlying first layer of conductive material prior to patterning; and
 forming the gate electrode such that the second layer of conductive material contacts the surface of the layer of conductive material in the selected region.

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European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 40 0823

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
X	EP-A-0 190 928 (TOSHIBA) * Whole document *	1, 18	H 01 L 21/28
Y		9	H 01 L 21/60
A		2-4, 6-8, 13-17, 20, 21	H 01 L 21/90

Y	EP-A-0 162 774 (DIGITAL) * Page 10, line 27 - page 13, line 18 *	9	
A		1, 4, 5, 11, 12, 15, 19, 20	

A	EP-A-0 176 010 (TEXAS INSTRUMENTS) * Figure 4 *	1, 4, 5, 9, 12, 15, 21	

A	NEUES AUS DER TECHNIK, no. 3/4, 15th August 1984, pages 1-2, Vogel-Verlag, Würzburg, DE; "Zonen mit Submikronbreite durch Schadenimplantation" * Whole article *	13, 14, 17, 18	

A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 3, August 1984, pages 1413-1414, New York, US; C.M. HSIEH: "Deep double-implanted LDD for reducing substrate current" * Whole article *	1, 3, 9, 13-15, 18	

The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 26-06-1989	Examiner PHEASANT N.J.
CATEGORY OF CITED DOCUMENTS			
X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document		T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document	

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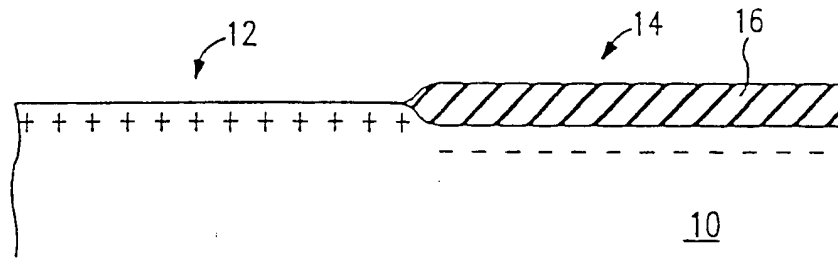


FIG. 1

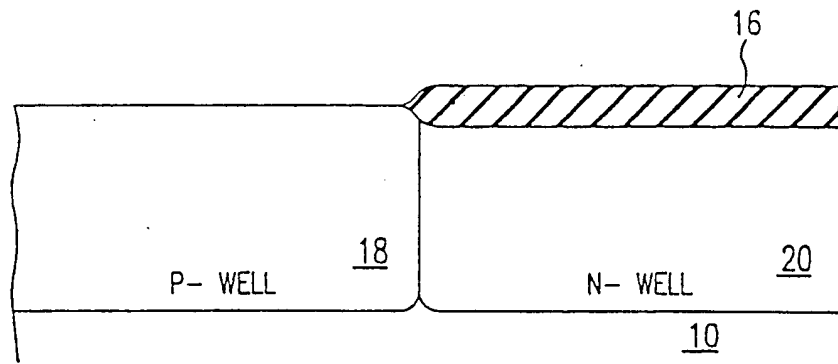


FIG. 2

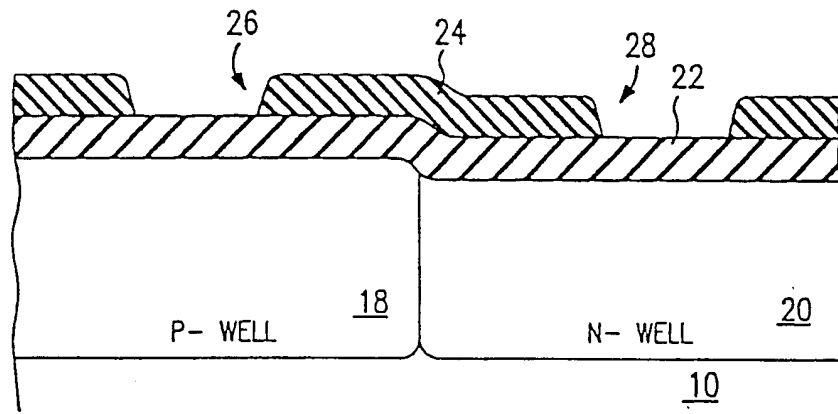


FIG. 3

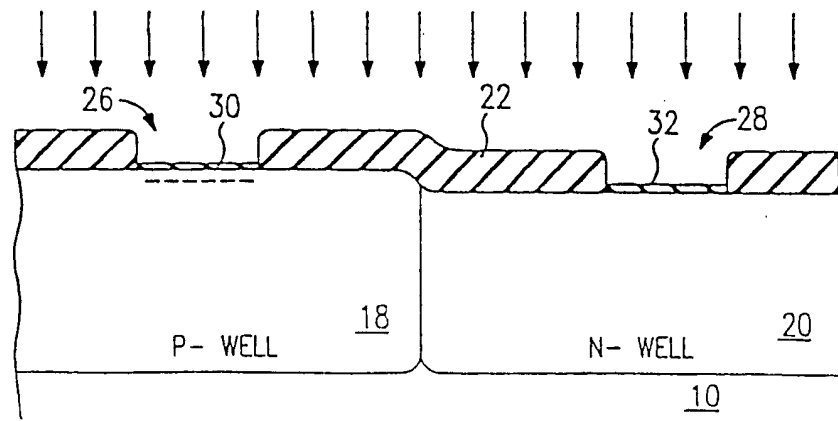


FIG. 4

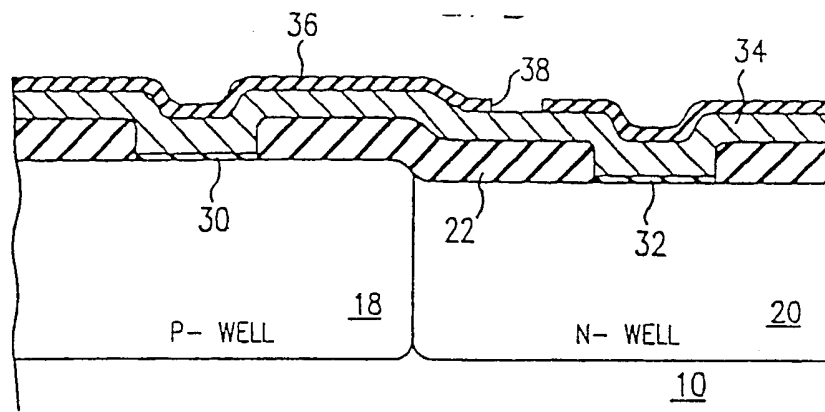


FIG. 5

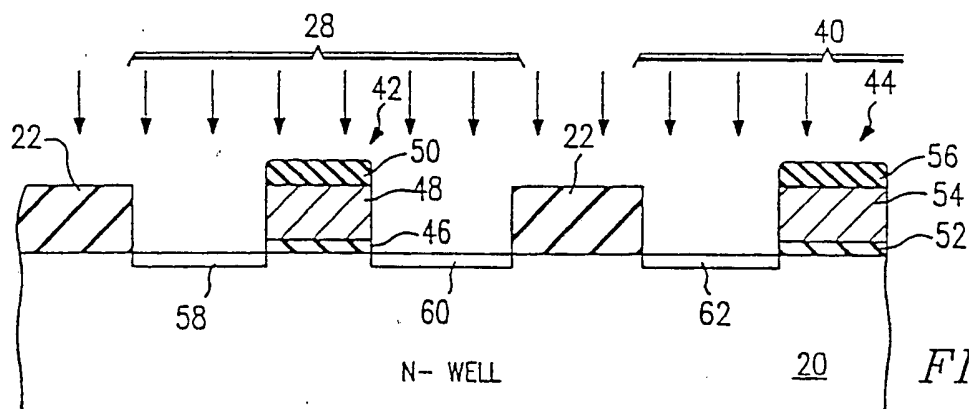


FIG. 6

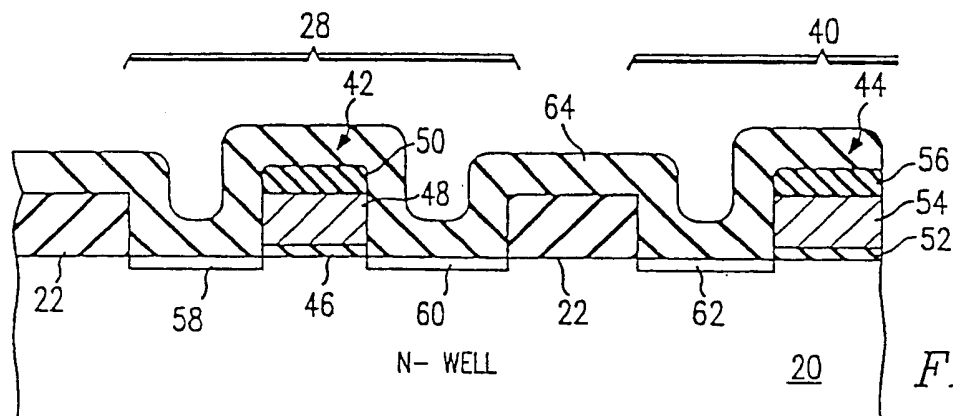


FIG. 7

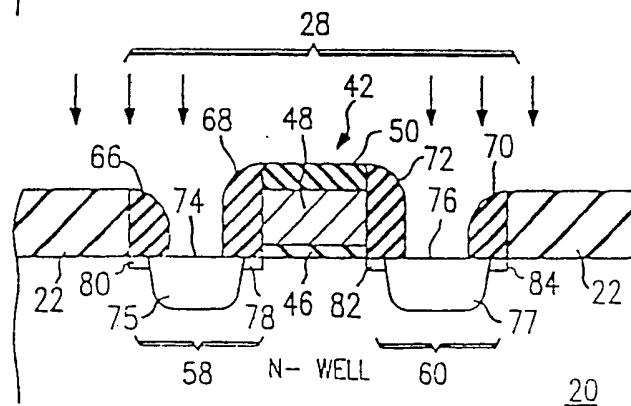


FIG. 8

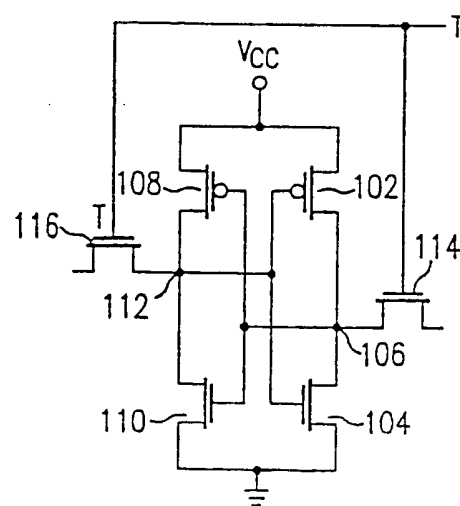
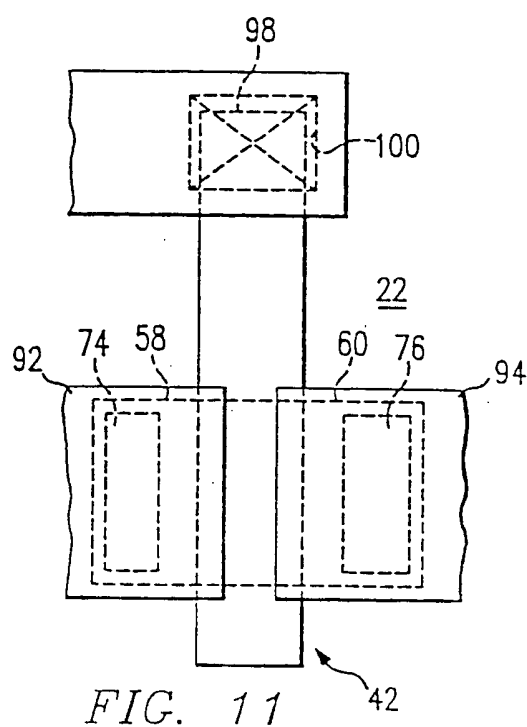
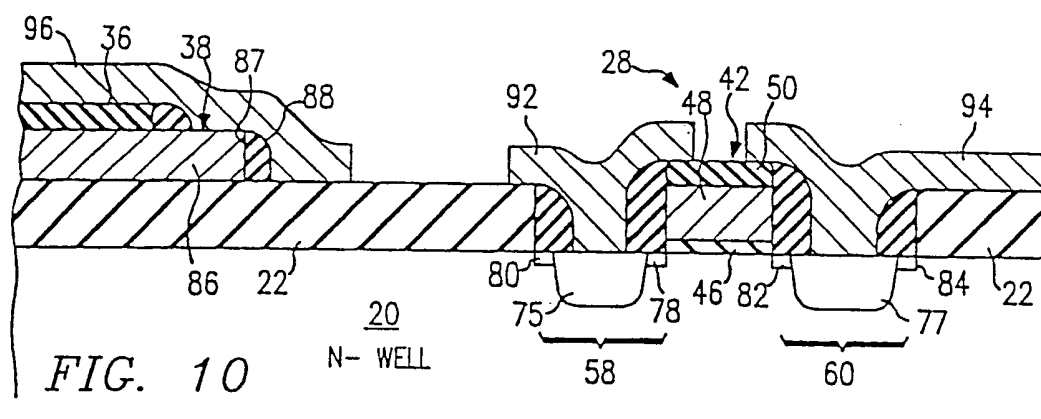
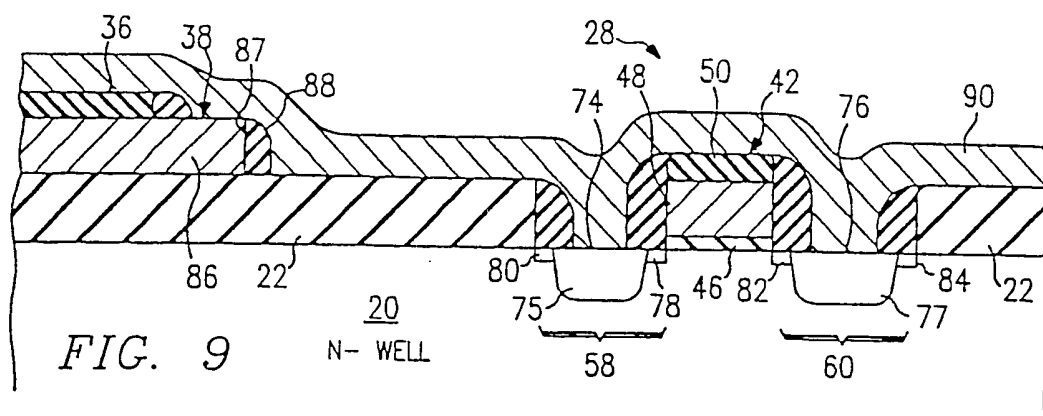


FIG. 12

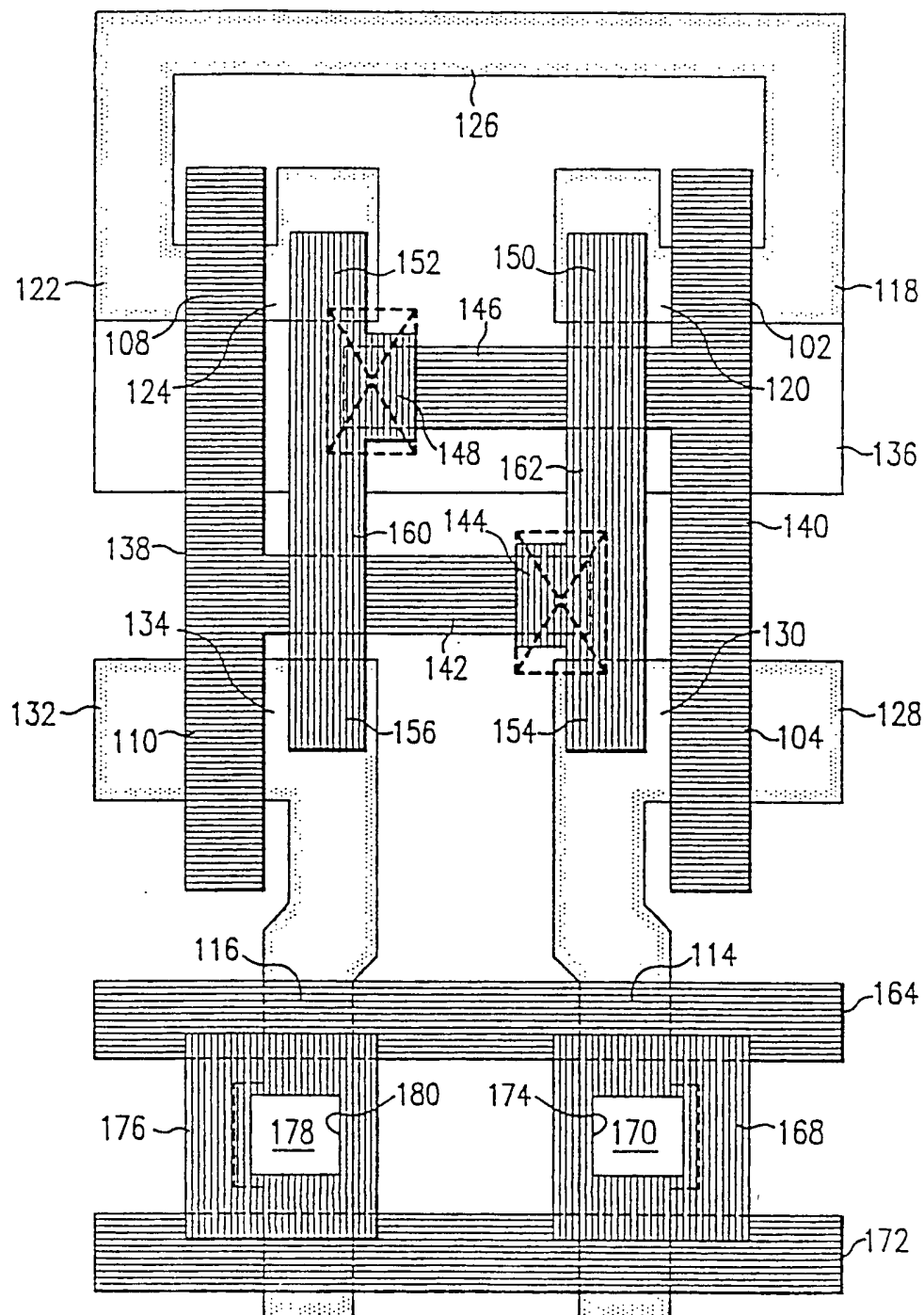


FIG. 13

